REMARKS

Claims 41-67 are pending in the present application.

In the office action mailed October 3, 2002 ("the Final Office Action"), claims 44, 49-53, 65-67 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,363,382 to Tsukakoshi ("the Tsukakoshi patent"). Claims 44, 49-53, 65-67 were also rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of U.S. Patent No. 5,659,737 to Matsuda ("the Matsuda patent"). Claims 44, 49-53, 65-67 are further rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of IBM technical disclosure bulletin entitled, Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory, June 1, 1988 ("the IBM technical disclosure").

A telephone conference with the Examiner and attorney of record was conducted on October 29, 2002. During the interview, the Examiner suggested several claim amendments believed to clarify language in the pending claims. Applicant considered the Examiner's suggestions and amended some of the claims accordingly. However, no agreement was reached with respect to allowable claims. As will be discussed below, it appears that the basis of the Examiner's rejection of claims 41-67 is based on an overly expansive reading of the teachings of the Tsukakoshi patent.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

In the Final Office Action, the Examiner went to great lengths to characterize the teachings of the Tsukakoshi patent as rendering the pending claims unpatentable. With respect to claims 41 and 45, the Examiner cited material from the Summary of the Invention, more specifically, col. 2, lines 13-50, as providing teachings that rendered claims 41 and 45 unpatentable. However, the Examiner's characterization of the teachings found in the cited material is inaccurate, and overly broad. The Examiner, at page 2, characterized the teachings of col. 2, lines 13-50 as follows:

> "***In other words***, in contrast to applicant's allegations on page 3 last para. [of the response to the Office Action mailed May 17, 2002], when memory cell [sic] is determined as defective, means is provided for substitution of address of said memory cell with a different address of non-faulty memory cell. Means is also provided, in col. 2 lines 35-50, for address compression, e.g., [citing to col. 2, lines 35-50]. Examiner does not understand how applicant fails to see or realize that address compression necessarily involves comparing means for subsequent memory access." (Emphasis in original.)

As illustrated by the Examiner's comments quoted above, the Examiner fails to understand the teachings of the Tsukakoshi patent. The Examiner appears to be under the mistaken belief that the Tsukakoshi patent teaches more than what the patent actually does. The Tsukakoshi patent simply teaches a system and method for exploiting an inherent characteristic of the design of redundant memory in a memory device which enables the use of a fault analysis memory (FAM) having a capacity that is less than that of the memory under test (MUT). This is explained in the language found in the Summary of the Invention, *see* col. 2, lines 35-50, and explained in greater detail at col. 3, line 50-col. 4, line 2. That is, as explained in Applicant's response to the Office Action mailed May 17, 2002, the Tsukakoshi patent teaches using a single cell in the FAM to represent "n" redundant rows or columns where n redundant rows or columns are replaced each time a redundant memory repair is made in the memory device. Given that the Tsukakoshi patent is directed to this purpose, the Tsukakoshi patent fails to describe various aspects of the combination of elements recited in the pending claims. For example, despite the Examiner's insistence, the Tsukakoshi patent does not teach a "means is provided for substitution of address of said memory cell with a different address of non-faulty memory cell." As previously described, a substitute address is not used in the system and method described in the Tsukakoshi patents. The failure flag stored by the FAM does not have a substitute address associated therewith. The flag is stored so that a redundant memory solution can be calculated to repair the memory device. Moreover, as will be explained in greater detail below, even if the Tsukakoshi teaches what the Examiner believes, the rejection of the claims cannot be supported because the Examiner fails to find teachings for each and every element of the combination of elements recited in the pending claims.

Additionally, the Examiner mischaracterizes the teachings of the Tsukakoshi patent. The Examiner merely quotes language from the Tsukakoshi patent, highlighting portions of the language in an attempt to support the rejection of pending claims. A "comparison means"

is underlined by the Examiner, in what is assumed to be the Examiner's attempt to imply that the comparison means disclosed by the Tsukakoshi patent is relevant to the limitations recited in the pending claims. However, as clearly stated in the quoted material, the role of the comparison means is for comparing *data*. Data comparison is not a limitation that is recited in any of the pending claims. Similarly, the Examiner underlines "address allocation" and "address compression" as if the discussion of the two in the Tsukakoshi patent is relevant. However, in reading the portion related to address allocation and address compression in the Tsukakoshi patent, it is evident that the discussion is not even remotely related to the subject matter, or more importantly, to the language of the pending claims. The address compression discussed in the Tsukakoshi patent is related to setting a flag of one memory cell in the FAM to represent failure of any one of multiple memory cells of the MUT. As previously discussed, the locations of all the defective memory cells of a MUT stored by the FAM are used to solve a redundant memory solution that can be used to repair the MUT using the redundant memory. There are no substitute addresses associated with the flags stored in the FAM, and the flags stored by the FAM are never compared with the memory addresses of a memory access request.

Applicant, however, wants to clarify that the Applicant's position is that the Tsukakoshi patent not only fails to teach what the Examiner purports the Tsukakoshi patent does, but more importantly, fails to teach *several* aspects of the *claimed* invention, and moreover, fails to teach the *combination* of elements recited by the pending claims. It appears that the Examiner has violated one of the cardinal rules in formulating a *prima facie* case of obviousness. As clearly held by the Federal Circuit, and as acknowledged in the Manual of Patent Examining Procedure (MPEP) at section 2142, a *prima facie* case of obviousness requires, among other things, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP, 8th Edition, section 2142, p. 2100-121. None of the Examiner's rejections of the pending claims even attempts to relate the teachings of the Tsukakoshi patent to any of the claim limitations recited in the pending claims. As demonstrated by the Examiner's arguments, which simply make generalizations about the teachings of the Tsukakoshi patent and the subject matter of the claims, the claim rejections are unsupportable because a *prima facie* case of obviousness is not established. .

For example, with respect to claims 41 and 45, at page 1 of the Final Office Action, the Examiner characterizes the material at col. 2, lines 13-25 of the Tsukakoshi patent as

generally teaching, "address signals," a "comparison means," an "address allocation means," "address allocation," and "address compression" sufficient to render claims 41 and 43 unpatentable. However, the Examiner fails to relate the purported teachings to the combination of limitations recited in claims 41 and 45. Additionally, the Examiner states that he "does not understand how applicant fails to see or realize that address compression necessarily involves comparing means for subsequent memory access." *See* page 3 of the Final Office Action. Without discussing the merits of the Examiner's statement, even if we assume that the statement is accurate for the sake of argument, the Examiner does not comment as to any of the other limitations recited in claim 41 and 45.

Claim 41 recites a method for accessing a memory, comprising comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format, the defective memory addresses having substitute addresses associated and stored therewith, where the memory address matches one of the decompressed defective memory addresses, extracting the substitute address associated therewith, and accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address. Claim 45 recites a method for accessing a memory device receiving memory addresses, the method comprising comparing the received memory addresses to decompressed addresses of defective memory locations in the memory device, the decompressed addresses of the defective memory locations otherwise stored in a compressed format having associated therewith substitute addresses corresponding to substitute memory locations in another memory, and substituting for the memory addresses matching the decompressed addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory.

Even if we assume for the sake of argument that the Examiner's characterization of the teachings of the Tsukakoshi patent are accurate, the Examiner ignores the language recited in the claims and fails to show how each of the limitations are disclosed by the description of the Tsukakoshi patent. For example, assuming that an "address compression necessarily involves comparing means for subsequent memory access," the Examiner still does not show where the Tsukakoshi patent describes, "comparing a memory address of *a memory access request* to decompressed defective memory addresses that are otherwise stored in a compressed format, *the defective memory addresses having substitute addresses associated and stored therewith*," as

recited in claim 41. The Examiner also fails to demonstrate that the Tsukakoshi patent teaches, "where the memory address matches one of the decompressed defective memory addresses, *extracting the substitute address associated therewith*," as also recited in claim 41. The Examiner also fails to demonstrate that the Tsukakoshi patent teaches, "*accessing a memory location corresponding to the extracted substitute address* rather than a memory location corresponding to the memory address," as further recited in claim 41.

With respect to claim 45, the Examiner fails to show where the Tsukakoshi patent teaches, "comparing *the received memory addresses* to decompressed addresses of defective memory locations in the memory device, the decompressed addresses of the defective memory locations otherwise stored in a compressed format *having associated therewith substitute addresses corresponding to substitute memory locations in another memory*," as recited in claim 45. The Examiner also fails to show where in the Tsukakoshi patent it is taught, "*substituting for the memory addresses* matching *the decompressed addresses of defective memory locations* the associated substitute memory addresses *to access the substitute memory locations in the other memory*," as further recited in claim 45.

Thus, even if we assume for the moment that the Examiner has not mischaracterized the teachings of the Tsukakoshi patent, the Examiner still nevertheless fails to establish a *prima facie* case of obviousness for the rejection of claims 41 and 45.

For the foregoing reasons, claims 41 and 45 are patentable over the Tsukakoshi patent. Therefore, the rejection of claims 41 and 45 should be withdrawn.

The previous discussion of the Tsukakoshi patent with respect to claims 41 and 45, similarly apply to claims 49, 54, 59, and 64. The rejection of claims 49, 54, 59, and 64 rely, in addition to the teachings of the Tsukakoshi patent, on various references cited by the Examiner as teaching power-on self testing (the Hoang patent), and the calculation of a value from the memory address comprising dividing the value represented by the memory address by a prime number or use of hashing code or function (the Meaden patent, the Matsuda patent, and the IBM technical disclosure). However, as stated in Applicant's response to the Office Action May 17, 2002, none of the references make up for the deficiencies of the Tsukakoshi patent. The combination of limitations recited by claims 49, 54, 59, and 64 are not disclosed, alone or in combination with the Hoang, Meaden, Matsuda patents, or the IBM technical disclosure, in the Tsukakoshi patent. The emphasis in the following text of claims 49, 54, 59, and 64, represent

just some of the limitations that the combined teachings of the Tsukakoshi patent and the secondary references cited by the Examiner fail to teach or suggest.

Claim 49 recites a method for accessing a requested memory location of a memory array, the requested memory location having a requested address, the method comprising generating a first hash code from the requested address, *comparing* the first hash code to hash codes *for decompressed addresses stored in a temporary memory array*, when a match is found between a hash code for a decompressed address and the first hash code, *determining if an address stored in the temporary array corresponds to the requested address*, and *accessing a spare memory array* when an address stored in the temporary array corresponds to the requested address.

Claim 54 recites a method for storing memory addresses of defective cells in a memory array, the method comprising receiving a memory test command, initiating a memory test in response to the memory test command, the memory test for determining memory addresses of defective memory cells of the memory array, *mapping memory addresses of defective memory cells to substitute addresses of substitute memory cells*, and compressing the memory addresses of defective memory cells *and the substitute addresses associated therewith.*

Claim 59 recites a method of remapping defective memory locations of a primary memory, the method comprising identifying memory addresses of the defective memory locations in the primary memory, *mapping* the identified memory addresses of the primary memory *to substitute memory addresses that correspond to substitute memory locations in a spare memory*, storing the identified memory addresses of the primary memory and the substitute memory addresses of the spare memory, and in response to a request to access a defective memory location in the primary memory, *substituting the associated substitute memory address in the spare memory for the memory address corresponding to the requested defective memory location in the primary memory.*

Claim 64 recites a method for accessing memory locations in a memory array, the method comprising steps of *determining whether a memory address matches an address of a defective memory cell*, the addresses stored in a temporary memory array, where a match is determined, *accessing a substitute memory location corresponding to a substitute memory address* associated and stored with the matching address, the substitute memory location located

in a separate memory array, and otherwise, access the memory location in the memory array corresponding to the memory address.

As previously discussed, it is obvious why the Examiner failed to find where the Tsukakoshi patent describes the combination of limitations of claims 49, 54, 59, and 64: the Tsukakoshi patent simply does not teach them, alone or in combination with the Hoang, Meaden, Matsuda patents, or the IBM technical disclosure. More specifically, there would not be any reason for the addresses of a memory access request to be compared with any address stored by the FAM. The obvious reason is that the Tsukakoshi patent does not contemplate comparing addresses of a memory access request, nor does the Tsukakoshi patent contemplate comparing *any* addresses against the defect flags in the FAM. The defective locations are stored in the FAM for the purpose of calculating a redundant memory solution that can be used to repair a MUT using redundant memory. Additionally, there are no substitute addresses associated and stored with the "compressed addresses" in the FAM (the Examiner's characterization of the defect flags, not the Applicant's) because the purpose of the FAM is to store defect locations for solving a redundant memory solution, not for address remapping purposes. There is also no substitution of addresses described in the Tsukakoshi patent because the information stored in the FAM are not the "addresses" of the defective locations, but merely flags that can be set which represent multiple memory cell locations, and then subsequently used to solve a redundant memory solution to repair the memory device. Accessing a substitute memory location associated with a substitute address is also not disclosed by the Tsukakoshi patent because, the purpose of the Tsukakoshi patent is providing a more efficient manner in which to store defective memory cell information for solving a redundant memory solution. Additionally, even if we assume that the Examiner's characterization of the Meaden and Matsuda patents, and the IBM technical disclosure is correct, it is uncertain how the particular compression algorithms described therein can be applied to the defect flags stored in the FAM as described in the Tsukakoshi patent. It is plain that the compressed addresses characterized as being stored in the FAM are nothing more than a single bit of information stored in a memory cell of the FAM that represent a plurality of memory cells on the MUT, one of which can be defective.

For the foregoing reasons, claims 49, 54, 59, and 64 are patentable over the combined teachings of the Tsukakoshi patent, in view of the Hoang, Meaden, or Matsuda

patents, or the IBM technical disclosure. Therefore, the rejection of claims 49, 54, 59, and 64 should be withdrawn.

Claims 42-44, which depend from claim 41, claims 46-48, which depend from claim 45, claims 50-53, which depend from claim 49, claims 55-58, which depend from claim 54, claims 60-63, which depend from claim 59, and claims 65-67, which depend from claim 64, are all patentable based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 42-44, 46-48, 50-53, 55-58, 60-63, and 65-67 should be withdrawn.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

All of the claims pending in the application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is requested to contact the undersigned at the number listed below for a telephone interview if, upon consideration of this amendment, the Examiner determines any pending claims are not in condition for allowance. The undersigned also requests the Examiner to direct all future correspondence to the address set forth below in the event the Examiner shows a different correspondence address for the attorney of record.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 41, 45-47, and 59-62 have been amended as follows:

41. (Once amended) A method for accessing a memory, comprising:

comparing a memory address of a memory access request to decompressed defective memory addresses that are otherwise stored in a compressed format, the defective memory addresses having substitute addresses associated and stored therewith;

where the memory address matches one of the decompressed [stored] defective memory addresses, extracting the substitute address associated therewith; and

accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address.

45. (Once amended) A method for accessing a memory device receiving memory addresses, the method comprising:

comparing the received memory addresses to decompressed addresses of defective memory locations in the memory device, the decompressed addresses of the defective memory locations otherwise stored in a compressed format having associated therewith substitute addresses corresponding to substitute memory locations in another memory; and

substituting for the memory addresses matching the decompressed addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory.

46. (Once amended) The method of claim 45 wherein the decompressed addresses of defective memory locations in the memory device are stored in a compressed format and wherein comparing the received memory addresses comprises decompressing at least one of the stored addresses of defective memory locations, and comparing a received memory address to the decompressed address.

47. (Once amended) The method of claim 45 wherein the decompressed addresses of defective memory locations in the memory device are stored in a compressed format and wherein comparing the received memory addresses comprises:

decompressing a portion of at least one of the stored addresses of defective memory locations;

calculating a value from a received memory address; and

comparing the calculated value to the decompressed portion.

59. (Once amended) A method of remapping [repairing a memory having] defective memory locations of a primary memory [therein], the method comprising:

identifying memory addresses of the defective memory locations in the primary memory [a respective defective memory address];

mapping the identified [defective] memory addresses of the primary memory to [associated] substitute memory addresses that correspond to substitute memory locations in a spare memory;

storing the identified [defective] memory addresses of the primary memory and the [associated] substitute memory addresses of the spare memory; and

in response to a request to access a defective memory location in the primary memory, substituting the associated substitute memory address in the spare memory for the memory address corresponding to the requested defective memory location in the primary memory.

60. (Once amended) The method of claim 59 wherein the primary memory having the defective memory locations comprises [are located in] a first memory device and the [substitute] spare memory [locations are located in a separate] comprises a second memory device.

61. (Once amended) The method of claim 59 wherein identifying the defective memory locations comprises testing all of the memory locations of the primary memory prior to accepting a first memory access request.

62. (Once amended) The method of claim 59, further comprising compressing the defective memory addresses and the [associated] substitute addresses prior to storing.